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CALL FOR PAPERS

ABSTRACT DEADLINE: NOVEMBER 1, 2005

REMINDER: *In fairness to all potential authors, late abstracts will not be accepted.*

MRS Symposium E: Gate Stack Scaling—Materials Selection, Role of Interfaces, and Reliability Implications

Future CMOS devices will require aggressive Tinv scaling for performance gain and reduced gate leakage for low power consumption. Traditional nitrided-SiO₂ (SiON) dielectrics have been scaled to a point where further physical scaling results in unacceptably high-leakage current and degrades carrier mobility in the channel. While effort is still ongoing to investigate scaling options for SiON dielectrics, a more intense effort is under way to find a high-*k* replacement for SiON dielectrics. Although the intuitive approach of replacing the gate dielectric alone with high-*k* dielectrics—while retaining the well-tested poly-Si electrodes—helps to reduce the gate leakage, it suffers from a host of issues. pFET gates in such stacks exhibit a large threshold voltage shift, and scalability of such stacks is questionable due to large poly-Si depletion (~ 0.3-0.5 nm). Replacing poly-Si with metal electrodes is attractive to overcome these impediments and meet high-performance technology targets. However, identifying Si-band edge p+ and n+ metals and integrating them in a CMOS flow poses enormous challenges. Other seemingly easy and elegant approaches like fully silicided gate electrodes have been stymied by lack of work-function control. Many of these challenges are centered on candidate materials selection, their processing, and the role of interfaces formed between the various layers, which dominate the final electrical behavior and reliability of the gate stack. Unlike more established Si-based dielectrics, metal-oxide-based high-*k* dielectrics are poorly understood. Due to the strong process-structure-property correlation in these dielectrics, they are prone to numerous defects arising from impurity incorporation, lack of thermal and chemical stability, oxygen vacancies, etc. Such defects have a significant impact on the reliability of gate stacks—in terms of lifetime (Tbd/Qbd) and threshold voltage stability (PBTI/NBTI). This symposium will focus on gaining fundamental insight into these critical issues. Contributions are solicited in the above and related areas that enhance fundamental understanding of future gate stack materials, structure, property interactions, and their impact on electrical properties and reliability.

Proposed session topics include, but are not limited to:

- Materials, deposition mechanisms, and precursor selection
- Chemical/thermodynamic stability of electrode/dielectric/semiconductor interfaces
- Kinetics of interface reactions and interface engineering
- Band-structure and work-function determination
- Impact of process integration on gate stack stability
- Nitridation mechanisms and other scalability approaches
- Atomic-scale structural characterization
- Metallic and gaseous diffusion through gate stacks
- Current leakage and mobility-detraction mechanisms
- Advanced electrical characterization techniques
- Charge trapping, NBTI, and defect-characterization techniques
- Reliability and impact of hot carriers

Invited speakers include: **Yasushi Akasaka** (SELETE), **Yves Chabal** (Rutgers Univ.), **M. Copel** (IBM), **P. Majhi** (Sematech), **P. Majhi** (Sematech), **J.W. McPherson** (Texas Instruments), **Manuel Quevedo Lopez** (Sematech), **L. Ragnarson** (IMEC, Belgium), and **Akiyoshi Uedono** (Univ. of Tsukuba, Japan).

Symposium Organizers

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